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Title of the Invention: "Interconnection Array Chip"

Claims:

(1) An interconnection array chip, characterized by that a single chip is provided thereon with a plurality of terminals on the periphery thereof, interconnection patterns connected with said terminals, and programmable switching elements connected to or between said interconnection patterns.

Brief Description of the Drawings:

Figure 1 is a schematic diagram illustrating an embodiment of the present invention; and

Figure 2 is a plan view illustraing an example of a PLA board composed of the embodiment of the interconnection array chip employed in conjuction with PLA array chips.

$a_1$-$a_n$, $b_1$-$b_n$, $c_1$-$c_n$, $d_1$-$d_n$, $e_1$-$e_n$, $f_1$-$f_n$... terminal, 10-1 - 10-n, 11-1 - 11-i, 12-1 - 12-m, 13-1 - 13-m... interconnection pattern, 14, 14-1 - 14-4... switching element, 21... substrate, 22-1 - 22-9... PLA array chip, 23-1 - 23-9... interconnection array chip.

…アレイチップを縦横両方向に交互になど、他の配列方法も可能である。

また、本発明の配線アレイチップを用いて結線を施すことのできるチップは、第2図のPLA以外の論理回路素子チップであってもよく、全く同様にしてチップ間の端子接続と配線アレイチップ内のスイッチング素子のプログラミングを施せばよい。

効果

以上のように本発明の配線アレイチップはスイッチング素子のプログラミングにより、論理回路素子等のチップ間に所望の任意の結線を施すことができるように構成されているので、この配線アレイチップを標準品として予め用意しておき、ユーザーの要請に応じて必要な論理回路素子等と共に配設し、チップ間の端子接続とスイッチング素子のプログラミングを施すことにより、所望の論理回路が短期間で製作でき、かつその論理回路、延いてはそれを用いる装置等のコストが低下するなどすばらしい効果を達成することができる。

4.図面の簡単な説明

第1図は本発明の一実施例を示す結線図、第2図は一実施例の配線アレイチップをPLAアレイチップと共に用いてPLAボードを構成した例を示す平面図である。

$a_1 \sim a_n$ ・$b_1 \sim b_n$ ・$c_1 \sim c_i$・$d_1 \sim d_i$・$e_1 \sim e_m$ ・$f_1 \sim f_m$ …端子、10-1～10-n，11-1～11-i．12-1～12-m．13-1～13-m…配線パターン、14，14-1～14-4…スイッチング素子、21…基板、22-1～22-9…PLAアレイチップ、23-1～23-9…配線アレイチップ。

特許出願人　株式会社　リコー

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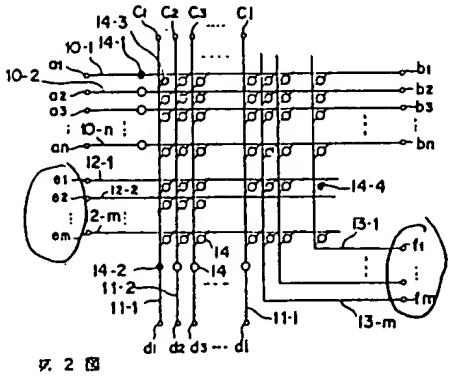
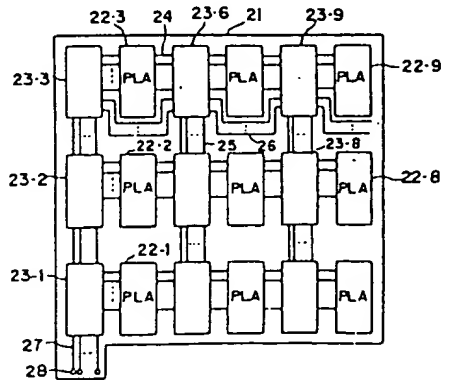
第1図




第2図



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# Wiring Array Chip

Application Number: 58-37167
Application Date: March 7, 1983

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SPECIFICATIONS:

1. Title of invention: Wiring Array Chip

2. Scope of the Claims of the Patent

(1) This invention relates to a wiring array chip, characterized ~~by~~ having 1 chip, provided with multiple terminals on the peripheral part of the chip, and wiring patterns connecting said terminals; wherein the wiring array chip is also provided with a programmable switching element, connected to said wiring patterns or in the area between said wiring patterns.

3. Detailed Explanation of the Invention

Sphere of Technology

This invention relates to a wiring array chip which is characterized by desired connections between any diagram elements.

Prior Art

Various devices that use multiple chips making up the configuration of logical circuit elements and PLA, (programmable array elements), must have wiring between individual chips. Since generally speaking a large number of processes is required to connect individual chips, the problems is that the assembly of such and similar devices is very time consuming and their cost is high.

Purpose

The purpose of this invention is to provide a general purpose standard wiring array chip which will enable desired connections of logical circuit elements, PLA, and similar elements that can be manufactured in a short period of time and inexpensively.

Structure

The following is an explanation of an application example of this invention. Figure 1 shows a simplified wiring diagram of 1 wiring array chip of an application example of this invention, formed on 1 chip.

Wiring pattern 10 - 1 to 10 - n is mounted between the terminals so as to correspond to input/output terminals for wiring

in the vertical direction of ($a_1$) - ($a_n$). Letters ($c_1$) - ($c_i$) and ($d_1$) - ($d_i$) stand for input\output terminals of wiring in the horizontal direction. Also in this case, the wiring pattern (11 - 1) - (11 - i) is mounted between the terminals. Symbols ($e_1$) through ($e_m$), and ($f_1$) through ($f_m$) indicate input terminals for a loop connection. The terminals for loop connection are connected to 1 wiring pattern (12 - 1) through (12 - m), and (13 - 1) - (13 - m). Each input\output terminal is located in the peripheral part of the chip.

[page 2]

The programmable switching element (14) is located in the crossing point between the horizontal wiring pattern (10 - 1) through (10 n) and the vertical wiring pattern (11 - 1) through (11 i), as well as between each of the wiring patterns (10 - 1) through (10 - n), (11 - 1) through (11 i), (12 - 1) through (12 m), and (13 - 1) through (13 m).

For this switching element (14) it is possible to use any bipolar transistor that is employed in PLA, and FAM, OS, or diode, electric or thermal conducting mode or non-conducting mode of the programmable element.

An application example of the wiring array of this invention can consist for instance of terminals ($a_1$) and ($b_1$) with connections between them in the horizontal direction, and the program can be executed in the conducting mode of the switching element (14 - 1). Also, to establish connections for instance between the terminals ($c_1$) and ($d_1$), the program can be executed in the conducting mode of the switching element (14 - 2). If, for instance, the switching element (14 - 3) is in the conducting mode, connection is established between the terminal ($c_1$) in the vertical direction and the element ($b_1$) in the horizontal direction. If, for instance, the switching element (14 - 4) is in the conducting mode, connection is established between the loop terminal ($e_1$) and ($f_1$). Thus it is possible to establish connection between desired terminals when suitable switching elements are in the conducting mode as shown above.

In this manner, the wiring array of this invention contains a configuration of 1 chip array, consisting of terminals, a wiring pattern connecting the terminals, and a switching element connected to the wiring pattern or between the wiring pattern. Thanks to this configuration, connection is possible between any desired element.

In order to use this wiring array chip for connections between the multiple logical circuit elements and other element chips, the logical circuit elements and other element chips are mounted together with this wiring array chip, and the terminals of both

chips are connected. Programming of the switching element inside the wiring array chip can be carried out either before or after connecting the terminals with the logical circuit elements and other elements.

The following is an explanation of an application example of the wiring array chip of this invention that uses the PLA board configuration, shown on Figure 2.

Number (21) is the substrate, and 9 PLA array chips (22) (22 - 1 through 22 - 9), as well as 9 wiring array chips (23) (23 - 1 through 23 - 9), are mounted on the substrate (21). Their mutual arrangement is shown on the figure. The horizontal direction shows the area between the adjoining PLA array chip and the wiring array chip, connected in the horizontal direction of the wiring pattern (24), while the vertical direction shows the area between adjoining wiring array chips in the vertical direction of the wiring pattern (25). In addition, wiring pattern (26), forming a loop, is mounted between the wiring array chip (23 - 3) and (23 - 6), and (23 - 6) and (23 - 9). The input/output terminal of this port is connected to the wiring array chip (23 - 1) through the wiring pattern (27).

The PLA board of this example has an arrangement of multiple standard PLA array chips (22), and multiple standard wiring chips (23), mounted on one substrate board. Between them is a standard PLA board connected first through wiring patterns (24), (25), and (26), which serve to execute programs with the PLA array chip (22) and wiring array chip (23), depending on what it is used for.

PLA is usually provided with a programmable AND array and OR array, or with a NOR array, and it is well known that it is possible to form any desired logical circuit by executing the program in each array. However, tne threshold of the capacity of 1 PLA depends on the number of input/output elements.

Since according to the PLA board of this example 3 PLA array chips (22 - 1) through (22 - 3), implemented with 3 wiring array chips (23 - 1) through (23 - 3), are allocated per input/output terminal (28) of the board substrate (21), the number of this input/output terminals (28) can be increased up to three times of the number of the input/output terminals of 1 PLA array chip (22).

Furthermore, it is also possible to implement a different method of arrangement, for instance a mutual vertical and horizontal arrangement of both array chips, since there is no need to be limited to the method of arrangement of the PLA array chip (22) and of the wiring array chip (23) that is shown on Figure 2.

Finally, it is also possible to establish connections by using the wiring array chip of this invention even if logical a circuit element chips that is different from the PLA shown on Figure 2 is used, by carrying out in the same manner the programing of the switching element in the wiring array chip and of the terminal connections between the chips.

Effect

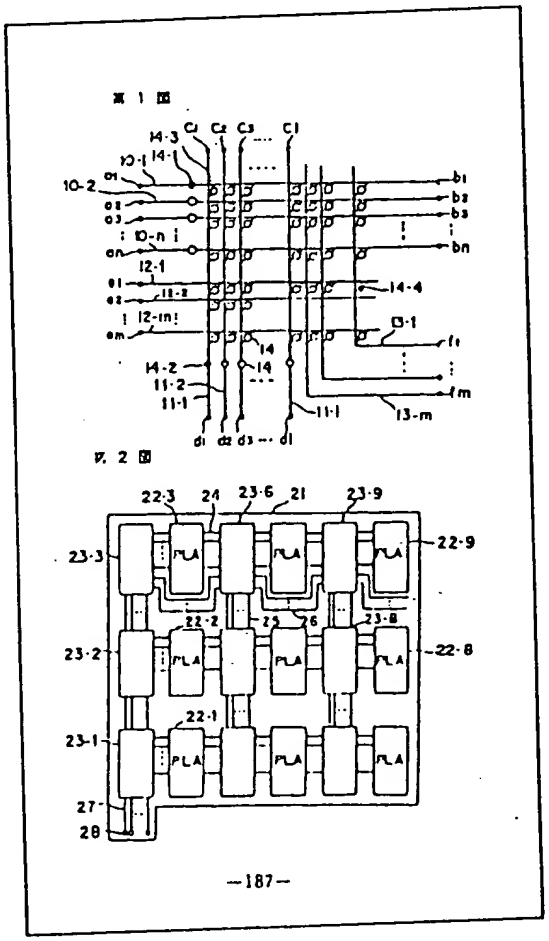
Since one can establish connection between any desired chips of the logical circuit elements and other chips depending on the programming of the switching element of the wiring array chip of this invention, such as the one mentioned above, it is possible first to manufacture this wiring array chip as a standard product, together with arrangements of required logic circuit elements and other elements depending on the requirements of the user. By carrying out programming of the switching element and of the connections between the chips, one can then manufacture in a short period of time desired logical circuits. Since this invention also permits to reduce the cost of devices required for such manufacturing, the effect that can be achieve is very significant.

## 4. Brief Explanation of Figures

Figure 1 shows a simplified wiring diagram of one application example of this invention, and Figure 2 shows a top view of a configuration of the PLA board, using a PLA board together with a PLA array chip of the wiring array chip of the application example.

Numbers ($a_1$ - $a_n$), ($b_1$ - $b_n$), ($c_1$ - $c_n$), ($c_1$ - $c_n$), ($d_1$ - $d_n$), ($e_1$ - $e_n$), and ($f_1$ - $f_n$), represent the terminals, (10 - 1) through (10 - n), (11 - 1) through (11 - i), (12 - 1) through (12 - i), (13 - 1) through (13 - m) represent the wiring pattern, (14) and (14 - 1) through (14 - 4) are switching elements, (21) is the substrate, (22 - 1) through (22 - 9) represents the PLA array chip, and (23 - 1) through (23 - 9) represents the wiring array chip.

Figure 1 and Figure 2



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